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Substitute for form 1449PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	Not Yet Assigned 10-736879
Filing Date	Herewith
First Named Inventor	Seongmoon wang
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	02008

Sheet 1 of 3

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁴
		Country Code ³ Number * Kind Code ² (if known)				

Examiner Signature	<i>Alvando</i>	Date Considered	3-17-06
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This collection of information is required by 37 CFR 1.97 and 1.53. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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		Art Unit	Not Yet Assigned
		Examiner Name	Not Yet Assigned
		Attorney Docket Number	02008
Sheet 2	of 3		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
TD	B	D. Belete, A. Razdan, W. Schwarz, R. Raina, C. Hawkins, and J. Morehead. Use of DFT Techniques In Speed Grading a 1GHz+ Microprocessor. In Proceedings IEEE International Test Conference, pages 1111-1119, 2002.	
	C	K.-T. Cheng, S. Devadas, and K. Keutzer. A Partial Enhanced-Scan Approach to Robust Delay-Generation for Sequential Circuits. In Proceedings IEEE International Test Conference, pages 403-410, 1991.	
	D	V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. Reddy. Techniques for Minimizing Power Dissipation In Scan and Combinational Circuits During Test Application. In IEEE Trans. on Computer-Aided Design of Integrated Circuit and System, Vol. 17(12), December 1998.	
	E	B. Dervisoglu and G. Stong. Design for Testability: Using Scanpath Techniques for Path-Delay Test and Measurement. In Proceedings IEEE International Test Conference, pages 385-374, 1991.	
	F	S. Gerstendorfer and H.-J. Wunderlich. Minimized Power Consumption for Scan-Based BIST. In Proceedings IEEE International Test Conference, pages 77-84, 1999.	
	G	M. J. Geuzebroek, J. T. van der Linden, and A. J. van de Goor. Test Point Insertion for Compact Test Sets. In Proceedings IEEE International Test Conference, pages 292-301, 2000.	
	H	P. Goel. An Implicit Enumeration Algorithm to Generate Tests for Combinational Logic Circuits. In IEEE Trans. on Computers, Vol. C-30(3), March 1981.	
	I	L. H. Goldstein and E. L. Thigpen. SCOAP: Sandia Controllability/Observability Analysis Program. In Proceedings IEEE-ACM Design Automation Conference, pages 190-196, 1980.	
	J	W. Mao and M. D. Ciletti. Reducing Correlation to Improve Coverage of Delay Faults In Scan-Path Design. In IEEE Trans. on Computer-Aided Design of Integrated Circuit and System, Vol. 13(5), May 1994.	
TD ✓	K	I. Pomeranz and S. M. Reddy. On Achieving Complete Coverage of Delay Faults In Full Scan Circuits using Locally Available Lines. In Proceedings IEEE International Test Conference, pages 923-931, 1999.	

Examiner Signature	<i>Amendo</i>	Date Considered	3/17/06
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.
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TD	L	J. Savir and R. Berry. At-Speed Test is not Necessarily an AC Test. In Proceedings IEEE International Test Conference, pages 722-728, 1991.	
	M	J. Savir and S. Patil. Scan-Based Transition Test. In IEEE Trans. on Computer-Aided Design of Integrated Circuit and System, Vol. 12(8), August 1993.	
	N	J. Savir and S. Patil. Broad-Side Delay Test. In Transactions on Computer-Aided Design of Integrated Circuit and System, Vol. 13(8), August 1994.	
	O	J. Saxena, K. M. Butler, J. Gatt, R. R. S. P. Kumar, S. Basu, D. J. Campbell, and J. Berech. Scan-Based Transition Fault Testing - Implementation and Low Cost Test Challenges. In Proceedings IEEE International Test Conference, pages 1120-1129, 2002.	
	P	G. L. Smith. Model for Delay Faults Based Upon Paths. In Proceedings IEEE International Test Conference, pages 342-349, 1985.	
	Q	N. Tamarapalli and J. Rajski. Constructive Multi-Phase Test Point Insertion for Scan-Based BIST. In Proceedings IEEE International Test Conference, pages 649-658, 1996.	
	R	J. A. Waicukauski, E. Lindbloom, B. K. Rosen, and V. S. Iyengar. Transition Fault Simulation. In IEEE Design & Test of Computers, pages 32-38, April 1987.	
	S	S. Wang and S. K. Gupta. DS-LFSR: A BIST TPG for Low Switching Activity. In IEEE Trans. on Computer-Aided Design of Integrated Circuit and System, Vol. 21(7), July 2002.	
TD	T	IEEE standard 1149.1-2001. IEEE Standard Test Access Port and Boundary-Scan Architecture. IEEE standard board, New York, N.Y., pps 1-119, 1990.	

Examiner Signature	Umano	Date Considered	3/17/06
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